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**UNITED STATES PATENT APPLICATION**

of

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for

**MOCVD PROCESS USING OZONE AS A REACTANT  
TO DEPOSIT A METAL OXIDE BARRIER LAYER**

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**BACKGROUND OF THE INVENTION**

**1. The Field of the Invention**

The present invention relates to the formation of a barrier layer on an integrated circuit during the fabrication thereof. More particularly, the present invention is directed to a process for depositing a metal oxide etch stop or diffusion barrier on a semiconductor substrate of an integrated circuit using MOCVD with ozone gas as an oxidant.

**2. Background of the Invention**

The movement toward the progressive miniaturization of semiconductor integrated circuits has resulted in increasingly compact and efficient semiconductor structures. This movement has been accompanied by an increase in the complexity and number of such structures aggregated on a single semiconductor integrated chip. As feature sizes are reduced, new problems arise which must be solved in order to economically and reliably produce the semiconductor devices that are situated upon semiconductor substrates. In the context of this document, the term "semiconductor substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term "substrate" refers to any supporting structure including but not limited to the semiconductor substrates described above. Including in the definition of semiconductor substrate are structures such as silicon-on-sapphire and silicon-on-insulator.

As an example, submicron features of the semiconductor devices in semiconductor manufacturing are now required and have necessitated the development of improved means of making contact with the various structures of the devices on the semiconductor substrate of the integrated circuit. The smaller and more complex devices are achieved, in part, by

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1 reducing feature sizes and spacing and by reducing the junction depth of regions formed in  
2 the semiconductor substrate. Among the features which are being reduced in size are the  
3 contact openings through which electrical contact is made to underlying active regions in the  
4 semiconductor devices. Another related feature being reduced in size is the via openings  
5 through which different structural layers on the integrated circuit are provided with electrical  
6 communication.

7 One problem that has arisen when making contact to the various isolated regions on  
8 an integrated circuit is controlling the selectivity with which a contact or via opening is  
9 etched. The goal in etching is to provide an opening that is of uniform width and that ends  
10 exactly to the surface of the region sought to be accessed without intruding upon the region.  
11 Unfortunately, the etchant materials have proven difficult to control, making it a challenge  
12 to prevent the resulting opening from being etched too widely or deeply.

13 A second problem that typically arises after the via or contact opening has been  
14 etched is that of preventing the metallization material from reacting with the underlying  
15 region to which is being provided electrical communication. Historically, device  
16 interconnections have been made with aluminum or aluminum alloy metallization.  
17 Aluminum, however, presents the problem of spiking at junctions when brought into contact  
18 with a silicon containing material. Junction spiking is the result of the dissolution of silicon  
19 into the aluminum metallization, as well as the dissolution of aluminum into the silicon  
20 containing material. Typically, when aluminum contacts the doped silicon of the region  
21 directly, the aluminum eutectically alloys with the silicon at temperatures as low or lower  
22 than 450° C. When such a reaction occurs, aluminum in the contact is often diffused into the  
23 silicon region from the contact, forming an alloy spike structure.

24 The resulting alloy spike structure is a sharp, pointed region enriched in aluminum.  
25 The alloy spikes can extend into the interior of the underlying silicon substrate from the  
26 boundary between the contact and the underlying region to cause unwanted short circuit

1 conduction. This particularly occurs when the underlying region is a junction in an active  
2 semiconductor device and is formed in an extremely shallow region of the substrate. When  
3 such an unwanted conduction occurs, the semiconductor device no longer operates properly.  
4 This problem is exacerbated with smaller device sizes, because the more shallow junctions  
5 are easily shorted, and because the silicon available to alloy with the aluminum metallization  
6 is only accessed through the small contact or via area, increasing the resultant depth of the  
7 spike. Furthermore, silicon in the region is often dissolved into the aluminum electrode,  
8 and there is a tendency for silicon thus dissolved into the electrode to be precipitated at a  
9 boundary between the electrode and the region as an epitaxial phase. This increases the  
10 resistivity across the contact.

11 A related problem exists when a doped region of silicon exists adjacent an undoped  
12 region, or when other doped and undoped regions must be located next to each other. When  
13 a region of silicon dioxide is laid above a doped region, for example, the silicon dioxide has  
14 a tendency to react with the dopant, depleting the dopant of the active region. As a further  
15 example, when an undoped region such as a polysilicon gate in a transistor is to be covered  
16 by doped oxide layer such as borophosphorosilicate glass (BPSG), a problem of the  
17 polysilicon assimilating the dopant of the oxide layer can occur.

18 As a solution to the problem of maintaining selectivity of the etch, it is known to  
19 deposit an etch stop barrier above the region that is to be isolated. A contact 10 being  
20 formed with a typical etch stop structure is shown in Figure 1. In the formation of contact  
21 10, a discrete region 14 is first formed within a semiconductor substrate 12. A polysilicon  
22 layer 15 is then formed over discrete region 14. An oxide layer 16 is then formed over  
23 polysilicon layer 15. A layer of photoresist 18 is applied, exposed over discrete region 14,  
24 and developed. A contact or via opening 20 is then etched through a masked opening in  
25 photo resist layer 18, polysilicon layer 15, and oxide layer 16. An etch stop layer 22 is  
26 formed from materials selected to be impervious to the etchant, and that can later be

The next step is metallization. This is typically achieved by the deposition of a metallization layer 42 such as aluminum using one of the various known methods, including

1 CVD, sputtering, and aluminum reflow. Barrier layer 38 acts as a barrier against the  
2 diffusion of metallization layer 42 into active region 34 and vice-versa. When used in a via  
3 opening the process is essentially the same as that for forming a contact, as discussed above.  
4 Figure 3 shows a second type of diffusion barrier used for separating adjacent regions on an  
5 integrated circuit. In Figure 3, a doped polysilicon gate structure 54 is isolated from an  
6 underlying silicon substrate 52 and an overlying oxide layer 56 by a diffusion barrier 58.

7 Many choices of materials to form barriers are known in the art. One type of barrier  
8 layer that is used is formed from metal oxide ceramic compounds. See Verhaar et al., above.  
9 Layers formed from such compounds are used as both etch stop and diffusion barriers. They  
10 are removed after layering with chemical etchant processes. The difficulty with using metal  
11 oxide ceramic compounds as a barrier layer arises in deposition of the material. In sputter  
12 deposition, the targets are expensive to provide, and it has been found that sputter depositing  
13 does not provide adequate step coverage for increasingly small contact and via openings.

14 Another method of forming barrier layers with metal oxide ceramic compounds that  
15 has been tried in the past is chemical vapor deposition using organometallic source materials  
16 (MOCVD). When using this process, a source such as dimethyl aluminum hydrate is reacted  
17 with diatomic oxygen gas at high temperatures to form a metal oxide solid such as aluminum  
18 oxide, substantially in the form  $Al_2O_3$ . The other reaction products are carried away in the  
19 form of gases such as dimethyl hydrate  $H(CH_3)_2$ , CO or  $CO_2$ , and diatomic hydrogen.

20 The MOCVD method has several inherent drawbacks. For instance, it has proven  
21 difficult to provide even step coverage of contact and via openings with this process. At high  
22 temperatures the source gas exhibits a low thermal surface mobility lifetime in that the  
23 organometallic source gas decomposes and reacts with the sides of the opening before  
24 reaching the bottom of the opening. This is a result of the high temperatures that are  
25 necessary to oxidize the source gas with diatomic oxygen gas. As a consequence, the  
26 openings must be formed with lower aspect ratios, hindering miniaturization efforts.

1 Another problem inherent to MOCVD barrier layer formation is the entrapment of  
2 carbon in the aluminum oxide film. The carbon reacts slowly with the diatomic oxygen gas,  
3 and layers of aluminum oxide are deposited over the carbon before it can be volatilized and  
4 carried away. Due to the trapping of carbon molecules and the incomplete reaction of the  
5 carbon, the barrier layer takes on the characteristics of aluminum carbide, which typically  
6 does not function as an etch stop barrier. Consequently, the resultant barrier has an inability  
7 to maintain selectivity and resistance to diffusion. The resultant barrier becomes  
8 compromised by the formation of pinholes at the locations where the carbon has been  
9 entrapped. The etchant or metallization material is then able to penetrate the resultant barrier  
10 layer due to the pinholes.

11 From the foregoing discussion, it can be seen that it would be an advance in the art  
12 to provide a process of forming an effective etch stop or diffusion barrier layer in an effective  
13 form, such as a metal oxide barrier layer. Such a process would be beneficial if metal oxide  
14 barrier layers can be formed with good step coverage, without entrapped carbon, and without  
15 the use of expensive targets known to sputter deposition processing.  
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## SUMMARY OF THE INVENTION

The present invention seeks to resolve the above and other problems which have been experienced in the art. More particularly, the present invention constitutes an advancement in the art by providing an improved method for creating a barrier layer on an integrated circuit during the fabrication thereof.

The present invention comprises a process for forming a metal oxide deposition barrier on a silicon substrate of an integrated circuit using MOCVD. Under the present invention, a vaporized metal is used as a source gas, preferably in the form of an organometallic compound, and gaseous ozone (O<sub>3</sub>) is reacted with the source gas to form a metal oxide film which can be used as an etch stop or diffusion barrier.

The first step of the process comprises forming a region on a semiconductor substrate that is to later be isolated from materials deposited in future processes. The layer may simply be a doped region on the silicon substrate, or it can be polysilicon or some other deposited, grown, or otherwise formed material. The next step depends on whether the barrier layer is to be an etch stop layer or a diffusion barrier.

When the barrier layer is to be an etch stop layer, the barrier layer is formed directly over the region to be isolated. This is done by disposing the silicon substrate in a reaction chamber and exposing it to the source gas and the ozone. This is typically done at a very low pressure and at temperatures that are lower than those commonly used in the art. A temperature of around 300° C is preferred, though higher temperatures will cause quicker reactions. The source gas and the ozone react together over the region, with the ozone replacing carbon bonds in the source gas. The ozone also volatilizes the other elements of the source gas, such as carbon and hydrogen. The chamber is then purged, and the silicon substrate is removed from the reaction chamber.

When the deposited barrier layer is to function as an etch stop, a oxide layer is typically formed over a region on the semiconductor substrate, followed by a masking a



1 photolithography process. It is then etched, with the etch being selectively shaped by the  
2 etch barrier. Since the reaction forms an etch stop barrier that is primarily aluminum oxide  
3 rather than aluminum carbide, the etch will be uncompromised by entrapped carbon and  
4 proper selectivity will be maintained.

5 When the barrier layer to be formed is to function as a diffusion barrier, it may be  
6 formed in two ways. It may be formed directly over a region on a semiconductor substrate,  
7 as where the region is to be isolated from a later layered material. Additionally, when  
8 intended to be part of a contact or via opening, an oxide layer is grown over the region, the  
9 region is masked and etched in a photolithography process, and a process is conducted as  
10 described above of inserting the silicon substrate into a reaction chamber and exposing it to  
11 both a source gas and ozone at a low atmosphere and low temperature. The low temperature  
12 allows a longer life and better sticking coefficient of the source gas, and enables the source  
13 gas to migrate down the surface of the contact or via sidewalls so as to react at the bottom  
14 of the contact or via opening, and thereby produce a more even layer having uniform step  
15 coverage. The contact or via opening may then be metallized by sputter or reflow of  
16 aluminum or other materials. The metal oxide diffusion barrier prohibits the interaction of  
17 the metallization material with the underlying region. This prevents spiking and other  
18 undesirable effects.

19 Thus, the present invention provides a novel process for using MOCVD to create  
20 a metal oxide etch stop or diffusion barrier. The created barrier layer will not be  
21 compromised by entrapped carbon therein, and will provide uniform step coverage when  
22 formed on a contact or via opening. Furthermore, the present invention has advantages over  
23 sputter deposition in that expensive target materials need not be used, and the high reactivity  
24 of the gaseous ozone at low temperatures provides for a more uniform step coverage.  
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**BRIEF DESCRIPTION OF THE DRAWINGS**

In order that the manner in which the above-recited and other advantages of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 is a perspective view of a contact utilizing a barrier layer an etch stop barrier.

Figure 2 is a perspective view of a contact utilizing a barrier layer as a diffusion barrier.

Figure 3 is a perspective view of a contact utilizing a barrier layer as a diffusion barrier to isolate a polysilicon gate from an oxide layer on a silicon substrate.

Figure 4 is a perspective view of a reaction chamber containing a silicon substrate on is formed a barrier layer according to the inventive process.

1                   DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

2                   The present invention comprises a process for forming a metal oxide barrier layer  
3 during fabrication of an integrated circuit using a organometallic chemical vapor deposition.  
4 process (MOCVD). The source gas is a vaporized metal containing compound. Ozone is  
5 employed as the oxidizing agent. The metal oxide film produced by the process of the  
6 present invention is more effective as a barrier layer due to the use of ozone as an oxidizing  
7 agent.

8                   Ozone is highly reactive at lowered energy states and is easily reacted at low  
9 temperatures with gaseous sources such as organometallic compounds. Ozone is used as the  
10 oxidizing agent in the inventive MOCVD process, and allows the MOCVD process to be  
11 conducted at low temperatures. This, in turn, has led to the formation of improved etch stop  
12 and diffusion barrier layers using ceramic metal oxides.

13                  The MOCVD process of the present invention involves a source gas which can  
14 comprise any metal-containing compound, but is preferably an organometallic gas. Even  
15 more preferably, the source gas of the present invention comprises a compound including at  
16 least one metal as well as both carbon and hydrogen. Examples of sources gases preferred  
17 for use with the present invention include aluminum trimethane, aluminum tetramethane,  
18 trimethyl aluminum hydrate, dimethyl aluminum hydrate, titanium tetramethane, and  
19 tantalum. The most preferred metal oxide barrier layer to be formed is aluminum oxide in  
20 the form of  $Al_yO_x$ , where  $y = 2$  and  $x = 3$ , though other stoichiometric compounds of the  
21 oxides of aluminum are contemplated. Other preferred metal oxide barrier layers are  
22 titanium oxide, tantalum oxide, ruthenium oxide, and molybdenum oxide.

23                  The resultant metal oxide barrier layer is used under the present invention for such  
24 purposes as an etch stop barrier, with respect to Figure 1, and as a diffusion barrier to prevent  
25 metallization material such as aluminum and aluminum alloys from reacting with the  
26 underlying active region, as described above in relation to Figure 2. The diffusion barrier

1 may also be used to prevent two adjacent doped and undoped regions from interacting as  
2 described with respect to Figures 3 and 4.

3 The production process of the integrated circuit in which the present invention is  
4 used typically comprises initially forming a discrete region as part of a semiconductor  
5 structure on a silicon substrate of an in-process integrated circuit. Typically, the discrete  
6 region will be a doped active region such as an N+ or a P+ region, or will be a region of  
7 polysilicon material on devices such as resistors, diodes, and transistors.

8 When the metal oxide barrier layer of the present invention is intended for use in  
9 isolating the discrete region from making contact with other structural layers deposited in  
10 later procedures, the barrier layer is deposited directly over the underlying region using the  
11 process of the present invention. Masking processes, as known in the art, may be employed  
12 to select the area for deposition. A second structural layer is then deposited.

13 When the barrier layer is intended to function as an etch stop layer over a discrete  
14 region, the metal oxide barrier layer is formed over the discrete region using the inventive  
15 process and is then covered with an oxide layer. A contact is then formed by masking,  
16 etching, and metallization, as described in relation to Figure 1, with the etch stop layer  
17 selectively determining the area of the etch.

18 When the barrier layer is to be used as a diffusion barrier to protect the active region  
19 from undesirable interaction with the composition of other layers, the barrier layer is first  
20 deposited in a contact opening using the process of the present invention. The contact  
21 opening is typically formed as described in relation to Figure 2 above. Metallization of the  
22 contact is then performed. The diffusion barrier deposited by the present invention prevents  
23 contact of the region with the metallization material, thereby effectively avoiding detrimental  
24 effects such as spiking from occurring.

25 When the integrated circuit is formed having multiple structural levels, the levels  
26 are typically electrically connected with the use of a via. Under the present invention, the

1 via can be formed using an etch stop layer and/or diffusion barrier in a manner similar to that  
2 of forming contacts, as described in relation to Figures 1 and 2.

3 When a discrete region is to be isolated from interdiffusion with an adjacent  
4 structural level, the metal oxide barrier layer of the present invention is used as a diffusion  
5 barrier, as described above in relation to Figures 3 and 4.

6 As an example of the process under the present invention of depositing the metal  
7 oxide barrier layer on a region to be isolated comprises the following steps. First, a region  
8 to be isolated by a barrier is formed by doping a portion of the silicon substrate, or growing  
9 or depositing a material on the silicon substrate, depending upon the device or structure  
10 being formed. If the barrier layer is to be an etch stop barrier, it will be deposited directly  
11 above the region as described with respect to Figure 1. If the barrier layer is to be a diffusion  
12 barrier in a contact or via, the contact or via opening will first be formed as as described  
13 with respect to Figure 2. The barrier layer is then formed, as shown in Figure 4, by placing  
14 the in-process integrated circuit 62 and the region therein to be isolated within a reaction  
15 chamber 64 such as a CVD chamber. Reaction chamber 64 is then evacuated to a pressure  
16 preferably of about .1 to about 1 torr. Lower pressures will affect the temperature and/or the  
17 amount of time required for the reaction. Reaction chamber 64 is typically heated.

18 The source gas and an inert carrier gas are then pumped into the reaction chamber.  
19 The source gas is shown being pumped in through a conduit 66 and the inert carrier gas is  
20 shown being pumped in through a conduit 68. The source and carrier gases can also be  
21 mixed before being pumped into reaction chamber 64. Ozone is also pumped into reaction  
22 chamber 64. In Figure 4, the ozone is shown being pumped in through a conduit 70. This  
23 causes a reaction to occur above the surface of integrated circuit 62 that forms a solid metal  
24 oxide film on the surface of the substrate over the discrete region that is to be isolated.

25 Chemical bonds between the metal and carbon groups in the organometallic source  
26 gas are replaced during the reaction with oxygen originating in the ozone oxidant. Carbon,

1 hydrogen, and other elements of the source gas are volatilized in the same reaction, typically  
2 by being oxidized by reaction with ozone. The volatilized source gases are then suctioned  
3 away from the surface of the integrated circuit 62, leaving the metal oxide solid film  
4 deposited thereon. The reaction is allowed to continue for a selected duration, after which  
5 the reactants are shut off, the reaction chamber is purged with an inert gas, and the silicon  
6 substrate is removed.

7 The process of the present invention can be conducted at a lower temperature than  
8 with conventional processes using oxygen as an oxidant, due to the high reactivity of ozone.  
9 Higher temperatures result in quicker reactions and uneven step coverage, as discussed  
10 above, whereas with lower temperatures, the carbon is more fully volatilized by the ozone  
11 and carried away from the surface before it can become entrapped in the metal oxide layer.  
12 Therefore, the metal oxide barrier layer is primarily metal oxide, which is not substantially  
13 compromised by entrapped carbon, and the integrity of the layer is maintained.  
14 Consequently, when the barrier layer functions as an etch stop, proper selectivity of the etch  
15 is maintained.

16 In the inventive process, the effectiveness of the organometallic source gas is  
17 extended by low temperatures of the reaction process. The low temperature of reaction  
18 lessens the propensity of the source gas to decompose and break down the chemical bonds  
19 thereof prematurely and without effectively reacting. When forming contacts or vias at  
20 lower temperatures, the source gas will have a higher sticking coefficient and will more  
21 readily migrate down the surface of the sidewalls of the contact or via opening to the bottom  
22 of the opening, where it will then react. The organometallic source gas at the bottom of the  
23 contact or via opening also reacts more fully at the lower temperature due to the highly  
24 reactive nature of the ozone. As a result, substantially all of the carbon bonds are replaced  
25 with oxygen, and a more uniform step coverage results. The uniform step coverage provides  
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1 the advantage of a more effective barrier layer resulting in higher yield rates. It also allows  
2 for a higher aspect ratio of the contact or via opening to be used.

3 As an example of the inventive process, a source gas such as aluminum trimethane  
4 is reacted with ozone to deposit a solid layer of aluminum oxide preferably in the form of  
5  $\text{Al}_2\text{O}_3$  on the surface of a region to be isolated. The carbon and hydrogen of the reactants  
6 will be effectively volatilized by the ozone, having been oxidized into an essentially  
7 vaporous state, and will then be easily removed from the surface of the silicon substrate and  
8 the reaction chamber. An effective metal oxide barrier layer will thereby be formed on the  
9 surface of the region being isolated. It should be noted that the aluminum oxide may be in  
10 other molecular forms, such as  $\text{Al}_2\text{O}_2$ , without changing the nature of the invention, but  
11 should be primarily an oxide rather than a carbide. The aluminum oxide may be removed  
12 after a contact or via opening is formed using an etchant that is selective to aluminum oxide.  
13 One etchant that could be used is a solution of about 85%  $\text{CH}_3\text{PO}_4$  at a temperature of about  
14  $60^\circ\text{C}$ .

15 A similar process would occur with a source of aluminum tetramethane, trimethyl  
16 aluminum hydrate, and dimethyl aluminum hydrate. If the desired barrier layer material is  
17 titanium oxide, the process could be undertaken using titanium tetramethane as a source gas.  
18 A tantalum oxide could also be formed using tantalum as a source. Additionally, ruthenium  
19 oxide and molybdenum oxide could be formed under the inventive process using  
20 conventional source gases. It will be evident to one skilled in the art that other forms of  
21 vaporous metal compounds could be used with this process to deposit an effective metal  
22 oxide barrier layer.

23 As a result of this process, an etch stop barrier layer in a contact or via opening can  
24 be formed that will not be compromised by materials such as carbon from an organometallic  
25 source gas. The resulting contact or via has an opening providing an efficient electrical  
26 connection and low contact resistance. A contact using a diffusion barrier layer will have



1 a more uniform step coverage, allowing for a high aspect ratios, and resulting in enhanced  
2 yield rates in fabrication.

3 The present invention may be embodied in other specific forms without departing  
4 from its spirit or essential characteristics. The described embodiments are to be considered  
5 in all respects only as illustrated and not restrictive. The scope of the invention is, therefore,  
6 indicated by the appended claims rather than by the foregoing description. All changes  
7 which come within the meaning and range of equivalency of the claims are to be embraced  
8 within their scope.

9 What is claimed and desired to be secured by United States Letters Patent is: